In the Claims:

Please amend claims 1, 2, 9, 6, 11, and 14 as follows:

1. (currently amended) A method for implementing breakpoint based performance measurement using a set of hardware counters for counting hardware events; said hardware counters being programmable for counting predefined programmable processor events; said predefined programmable processor events including processor cycles and cache misses; said method comprising:

inserting a start breakpoint instruction and a stop breakpoint instruction in hardware instructions;

executing said hardware instructions and suspending processing of said hardware instructions responsive to executing said start breakpoint instruction;

responsive to executing said start breakpoint instruction generating a processor interrupt for entering interrupt handler instructions and calling breakpoint instructions;

said breakpoint instructions generating a start processing instruction to return processing from said interrupt handler instructions to the hardware instructions and ~~to start~~ starting said defined set of hardware counters, responsive to said generated start processing instruction; and

executing the hardware instructions and suspending processing of the hardware instructions and stopping said defined set of hardware counters, responsive to executing said end breakpoint instruction ~~to stop said defined set of hardware counters~~.

2. (currently amended) A method for implementing breakpoint based performance measurement as recited in claim 1 wherein said predefined processor

events further include at least one of processor instructions executed, ~~cache misses~~, a defined type of processor instruction executed, and translation lookaside buffer misses.

3. (original) A method for implementing breakpoint based performance measurement as recited in claim 1 wherein a user specifies, via a debugger breakpoint manager including a performance measurement program and a user interface, a start bound and an end bound of a performance collection region of a user source code and said set of hardware counters.

4. (original) A method for implementing breakpoint based performance measurement as recited in claim 1 wherein the inserting step includes inserting said start breakpoint instruction and said stop breakpoint instruction at arbitrary user defined locations in said hardware instructions.

5. (original) A method for implementing breakpoint based performance measurement as recited in claim 1 includes the steps of enabling a user to interrogate a program state and to request said start processing instruction.

6. (currently amended) Apparatus for implementing breakpoint based performance measurement comprising:

a plurality of hardware counters for counting hardware events; said hardware counters being programmable for counting predefined programmable processor events; said predefined programmable processor events including processor cycles and cache misses;

a source level debugger including a breakpoint manager;

said breakpoint manager including a performance measurement program and a

user interface;

said breakpoint manager utilizing said performance measurement program and said user interface for defining a set of said hardware counters for counting user specified ~~hardware~~ programmable processor events and for inserting a start breakpoint instruction and a stop breakpoint instruction in hardware instructions;

user program means for executing said hardware instructions and suspending processing of the hardware instructions responsive to executing said start breakpoint instruction and generating a processor interrupt for entering interrupt handler instructions and for calling said breakpoint manager;

said breakpoint manager for generating a start processing instruction to return processing from said interrupt handler instructions to the hardware instructions and ~~to start~~ starting said defined set of hardware counters, responsive to said generated start processing instruction; and

said user program means for executing the hardware instructions and suspending processing of the hardware instructions and stopping said defined set of hardware counters, responsive to executing said end breakpoint instruction ~~to stop said defined set of hardware counters~~.

7. (original) Apparatus for implementing breakpoint based performance measurement as recited in claim 6 wherein start breakpoint instruction includes encoded information specifying said defined set of hardware counters.

8. (original) Apparatus for implementing breakpoint based performance measurement as recited in claim 6 wherein said breakpoint manager, responsive to said

start breakpoint instruction, records user information specifying said defined set of hardware counters.

9. (currently amended) Apparatus for implementing breakpoint based performance measurement as recited in claim 6 wherein said predefined processor events further include at least one of processor instructions executed, ~~cache misses~~, a defined type of processor instruction executed, and translation lookaside buffer misses.

10. (original) Apparatus for implementing breakpoint based performance measurement as recited in claim 6 wherein said breakpoint manager inserts said start breakpoint instruction and said stop breakpoint instruction at arbitrary user defined locations in said hardware instructions.

11. (currently amended) A computer program product for implementing breakpoint based performance measurement in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

defining a set of hardware counters for counting hardware events; said hardware counters being programmable for counting predefined programmable processor events; said predefined programmable processor events including processor cycles and translation lookaside buffer misses;

inserting a start breakpoint instruction and a stop breakpoint instruction in hardware instructions;

executing said hardware instructions and suspending processing of said hardware instructions responsive to executing said start breakpoint instruction;

responsive to executing said start breakpoint instruction generating a processor interrupt for entering interrupt handler instructions and calling breakpoint instructions;

said breakpoint instructions generating a start processing instruction to return processing from said interrupt handler instructions to the hardware instructions and ~~to start~~ starting said defined set of hardware counters, responsive to said generated start processing instruction; and

executing the hardware instructions and suspending processing of the hardware instructions and stopping said defined set of hardware counters, responsive to executing said end breakpoint instruction ~~to stop said defined set of hardware counters~~.

12. (original) A computer program product for implementing breakpoint based performance measurement as recited in claim 11 includes the step of receiving user selections for a start bound and an end bound of a performance collection region of a user source code program and said set of hardware counters.

13. (original) A computer program product for implementing breakpoint based performance measurement as recited in claim 11 wherein the inserting step includes inserting said start breakpoint instruction and said stop breakpoint instruction at arbitrary user defined locations in said hardware instructions.

14. (currently amended) A computer program product for implementing breakpoint based performance measurement as recited in claim 11 wherein said predefined processor events include at least one of processor instructions executed, cache misses, and a defined type of processor instruction executed~~, and translation lookaside buffer misses~~.